What is claimed is:

1. An algorithmic analog-to-digital converter (ADC) comprising:

a sample-and-hold circuit; and

one ADC processing unit, wherein the sample-and-hold circuit and the ADC processing unit operate in parallel and share a single operational amplifier.

2. An algorithmic ADC as claimed in claim 1, wherein the ADC processing unit comprises a multiplying digital-to-analog converter (MDAC) and a sub-ADC.

3. An algorithmic ADC as claimed in claim 2, wherein the sample-and-hold circuit is integrated with the MDAC.

4. An algorithmic ADC as claimed in claim 3, wherein the MDAC comprises capacitors that are switchable between a sampled or residue voltage, and reference voltages.

5. An algorithmic ADC as claimed in claim 4, wherein the sub-ADC generates switch control signals that determine the reference voltages to be applied to the MDAC capacitors.

6. An algorithmic ADC as claimed in claim 5, and further comprising a clock generator, the clock generator generating a sample-and-hold clock and an ADC clock that

is N times faster than the sample-and-hold clock to define N ADC clock cycles per sample-and-hold clock period.

7. An algorithmic ADC as claimed in claim 6, wherein a triplet of data bits is generated by the ADC processing unit during at least one ADC clock cycle, adding the N triplets of data bits to generate the digital output stream of the algorithmic ADC.

8. An algorithmic ADC as claimed in claim 7, wherein N=5 to define five ADC cycles per sample-and-hold clock period, five triplets of data bits being added per sample-and-hold clock period to generate an 11-bit digital output per analog input sample.

9. An algorithmic ADC as claimed in claim 6, wherein each ADC clock cycle is further sub-divided into two phases, wherein during one phase the capacitors are switched coupled to a residue or sampled voltage provided by the MDAC, and during another phase the capacitor are coupled to a reference voltage determined by the switch control signals generated by the sub-ADC.

10. A video encoder chip comprising an algorithmic ADC as claimed in claim 1.

11. A video decoder chip comprising an algorithmic ADC as claimed in claim 1.

12. A set top box comprising an algorithmic ADC as claimed in claim 1.

13. An electronic appliance comprising an algorithmic ADC as claimed in claim 1.

14. A method for converting an input analog signal to an output digital bit stream, comprising:

sampling and holding the input analog signal during a sample-and-hold clock period;

generating N sets of bits during the sample-and-hold clock period using an ADC unit comprising one MDAC and one sub-ADC, wherein the N sets of bits are generated by alternately applying a residue or sampled voltage and a reference voltage to switched capacitors in the MDAC; and

generating the output digital bit stream by adding the N sets of bits.

15. A method as claimed in claim 14, wherein a single operational amplifier is used to sample and hold the input analog signal and to apply a residue or sampled voltage to the switched capacitors.

16. A method as claimed in claim 14, wherein five (N=5) sets of bits are generated per sample-and-hold-clock period to yield an 11-bit output digital bit stream when the five sets of bits are added.

17. A method for converting an input analog signal to an output digital bit stream, comprising:

a step for sampling and holding the input analog signal during a sample-and-hold clock period;

a step for generating an ADC clock having N cycles per sample-and-hold clock period;

a step for generating an intermediate analog voltage per cycle using the sampled analog signal and residue voltages derived from the sampled analog signal;

a step for generating a set of data bits per cycle from the intermediate analog voltage;

a step for generating feedback signals for generating the intermediate analog voltage in the next cycle; and

a step for generating the output digital bit stream using the N sets of data bits.

18. A method as claimed in claim 17, wherein each cycle is further divided into two phases, and wherein during a first phase a sampled analog signal or residue voltage is applied to switched capacitors, and wherein during a second phase reference voltages are applied to the switched capacitors.

19. A method as claimed in claim 18, wherein the feedback signals determine what reference voltages are applied to the switched capacitors.

20. A method as claimed in claim 19, wherein N=5 and five triplets of data $d_{\{0,1,2\}}^{I}$, $d_{\{0,1,2\}}^{II}$, $d_{\{0,1,2\}}^{III}$, $d_{\{0,1,2\}}^{IV}$ and $d_{\{0,1,2\}}^{V}$ are generated per sample-and-hold clock period.

21. A method as claimed in claim 20, wherein an output digital bit stream b[10:0] is generated by applying the digital reconstruction algorithm

$$\begin{array}{ccccccccccc} d_2^{I} & d_1^{I} & d_0^{I} & & d_2^{III} & d_1^{III} & d_0^{III} & & d_2^{V} & d_1^{V} & d_0^{V} \\ & & & d_2^{II} & d_1^{II} & d_0^{II} & & d_2^{IV} & d_1^{IV} & d_0^{IV} & + \\ \hline b_{10} & b_9 & b_8 & b_7 & b_6 & b_5 & b_4 & b_3 & b_2 & b_1 & b_0 \end{array}$$

to the five triplets of data.

22. A method as claimed in claim 18, and further comprising a step for correction of errors using the redundant signed digit (RSD) algorithm.

23. A system for conversion of an analog input signal to an output digital bit stream comprising:

means for sampling and holding an input analog signal;

means for applying the sampled and held signal to a switched capacitor circuit;

means for generating a residue voltage with the switched capacitor circuit;

means for generating N sets of data bits from the residue voltage per sampled and held signal; and

means for generating feedback signals corresponding to the data bits to control reference voltages applied to the switched capacitor circuit.

24. A system as claimed in claim 23, wherein the means for sampling and holding an input signal, means for applying the sampled and held signal to a switched capacitor circuit, and means for generating a residue voltage comprise a single operational amplifier.

25. A system as claimed in claim 23, wherein the means for generating N sets of data bits comprises a sub-ADC having a flash architecture.

26. A system as claimed in claim 25, wherein the switched capacitor circuit is contained within an MDAC, and a sample-and-hold circuit is integrated in the MDAC.

27. A system as claimed in claim 26, and further comprising clock generation means for generating a first clock governing operation of the sample-and-hold circuit and a second clock governing operation of the MDAC and sub-ADC.

28. A system as claimed in claim 27, wherein the second clock is N times faster than the first clock.